IN THE CLAIMS:

Please amend the claims pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked-up" version):

1. (Amended) A timing control device for the compensation of timing errors in multiple channel devices comprising at least one register, the device comprising:

a clock for providing a common clock signal to each said at least one register;

a reference signal generator for providing a reference signal applicable through a reference channel to said at least one register, for deskewing the register's channels with respect to said reference signal;

wherein for each said at least one register a corresponding feedback loop is associated for the relative alignment of register's channels timing in relation to the reference signal, said feedback loop comprising

a means for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence of symbols transmitted through the reference channel; and

a set of delay means which uses the determined information on deviation from the predetermined level of said probability to generate a feedback signal to compensate timing errors in said register.

3. (Amended) A timing control device for the compensation of timing errors in multiple channel devices comprising at least one register, the device comprising:

a clock for providing a clock signal to said at least one register;

a reference signal generator for providing a reference signal applicable through a reference channel to said at least one register, for deskewing the register's channels with respect to said reference signal;

wherein for each said at least one register a corresponding feedback loop is associated for the relative alignment of register's channels timing in relation to the reference signal, said feedback loop comprising

a means for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence of symbols transmitted through the reference channel;

a set of delay means which uses the determined information on deviation from the predetermined level of said probability to generate a feedback signal to compensate timing errors in said register; and

a modulator signal applied to the reference signal for obviating the timing hysteresis within the register.

22. (Amended) A self calibrating receiver comprising:

a register having a plurality of channels having inputs and outputs;

a clock means for providing a clock signal to the register;

a reference signal generator connectable to the input of at least one said channel of said register for supplying reference signals for deskewing the register;

a detecting means connectable to the output of at least one said channel of said register for detecting a deviation from a predetermined level of probability of reading by said

register from said reference channel a desired symbol on a boundary of two reference channel symbols in a sequence;

wherein the output of the detecting means is connectable to a set of delay means which uses the information received by said detecting means to generate a feedback signal to compensate timing errors in said register; and

a modulator signal is applied to the reference signal for obviating the timing hysteresis within said register.

43. (Amended) A method for the compensation of timing errors in multiple channel devices comprising at least one register, the method comprising the steps of:

providing a common clock signal to each said at least one register;

providing reference signals for deskewing the register;

detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence; and

generating for each said register a feedback signal using the determined information on deviation to compensate timing errors in said register until the clock reaches a zero skew with respect to the reference signal.

47. (Amended) A method for the compensation of timing errors in multiple channel devices comprising at least one register, the method comprising the steps of:

providing a clock signal to said register;

providing reference signals for deskewing the register;

detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence;

generating for each said register a feedback signal using the determined information on deviation to compensate timing errors in said register until the clock reaches a zero skew with respect to the reference signal; and

supplying a modulator signal applied to the reference signal for obviating the timing hysteresis within the register.